FIG. 1A

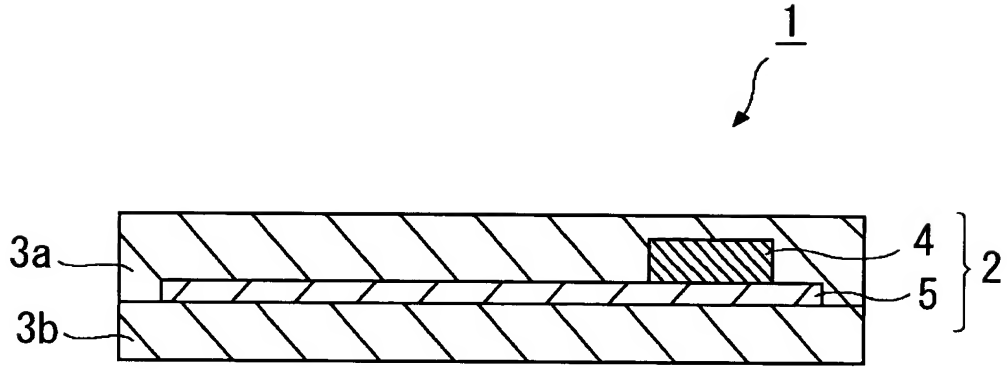


FIG. 1B

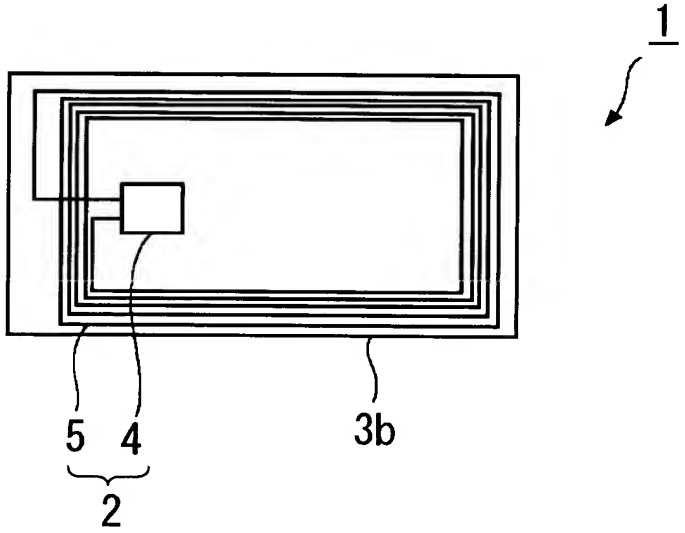


FIG. 2A

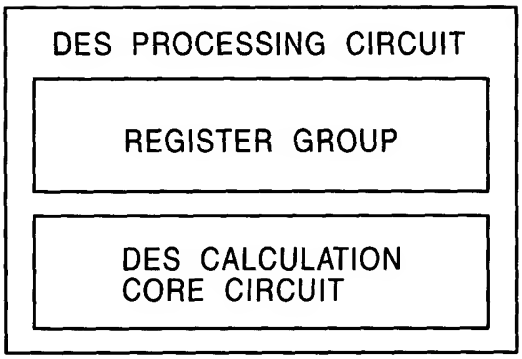


FIG. 2B

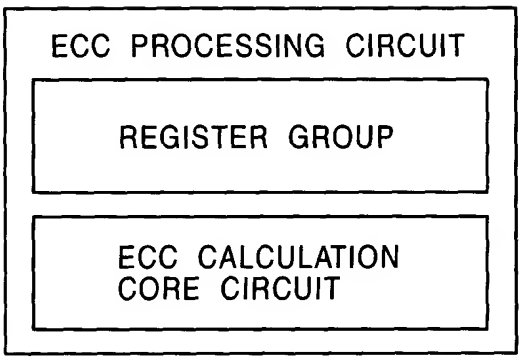


FIG. 2C

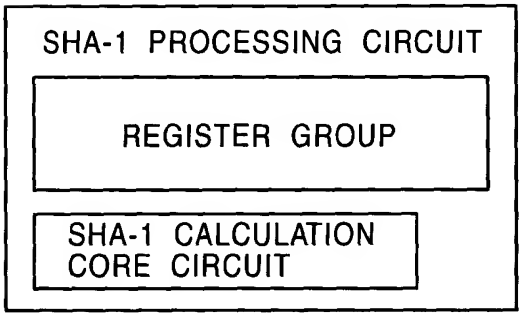


FIG. 2D

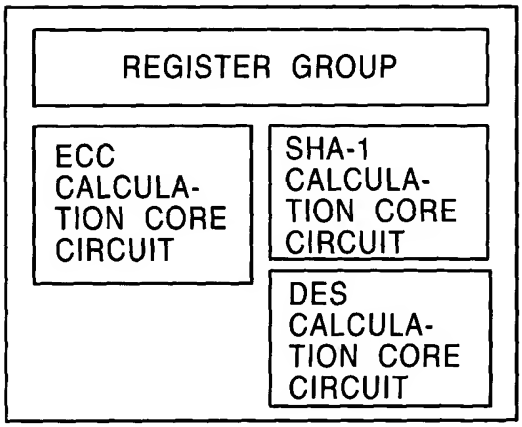


FIG. 3

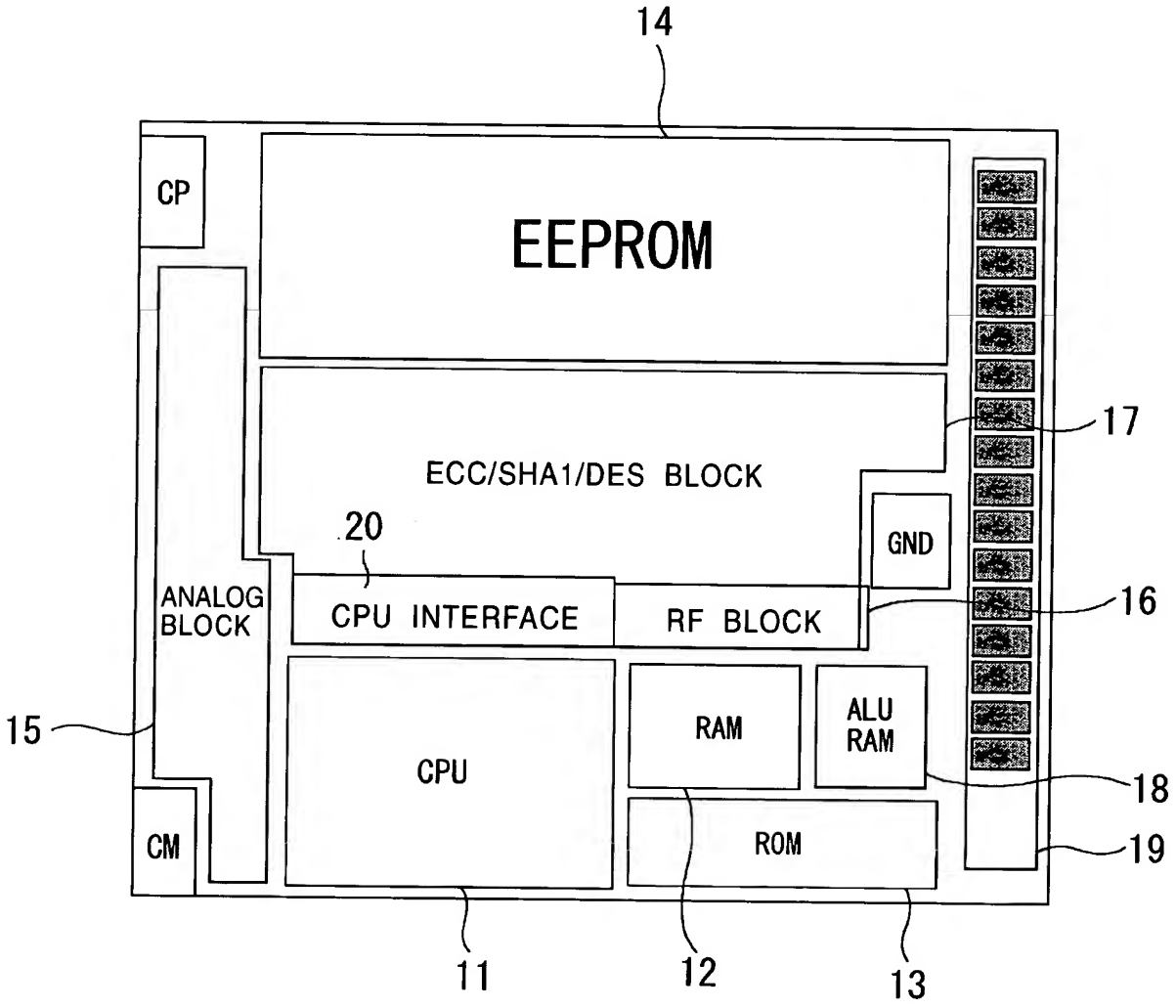
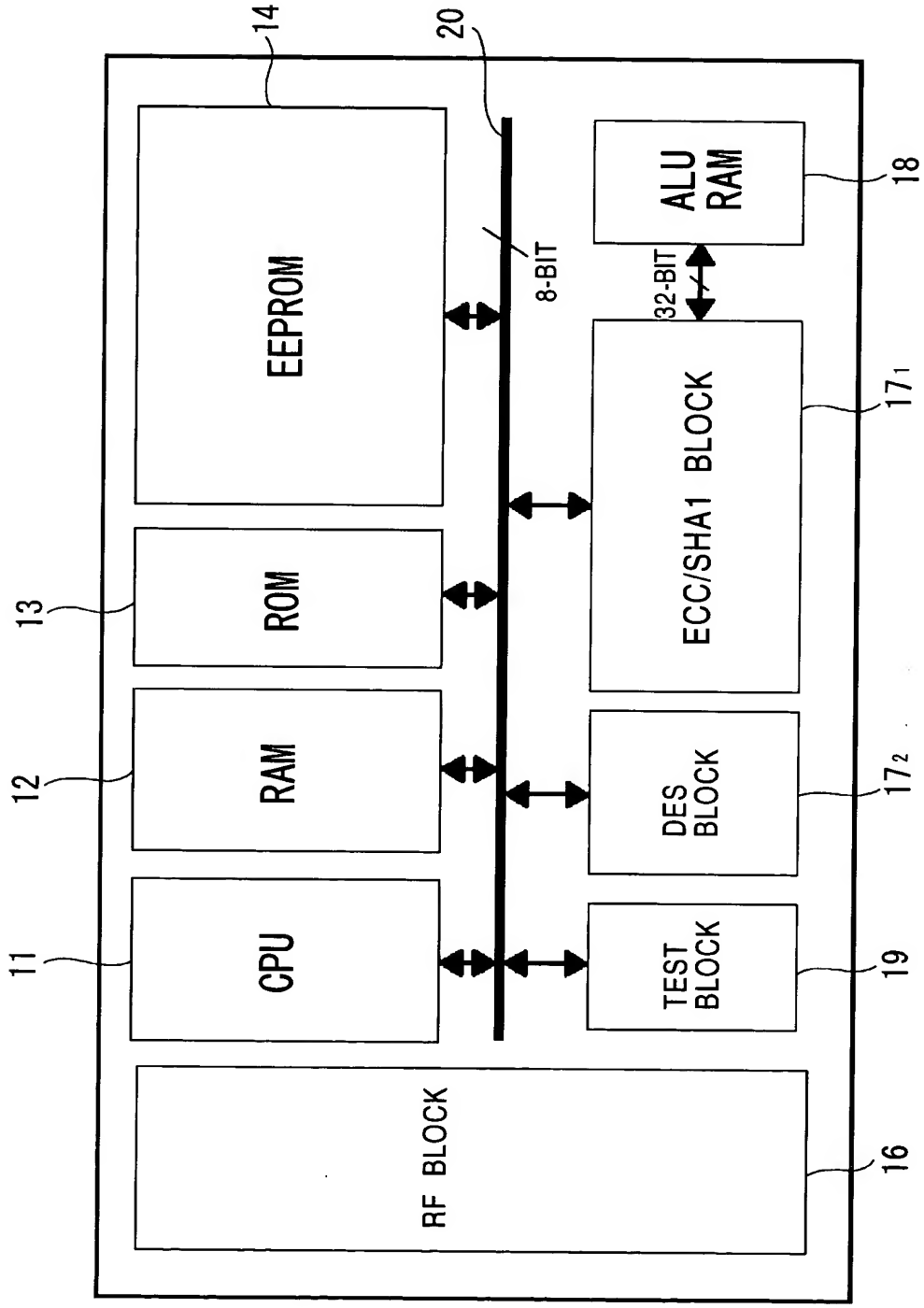

14
CP
EEPROM
17
ECC/SHA1/DES BLOCK
20
GND
ANALOG BLOCK
CPU INTERFACE
RF BLOCK
16
15
CPU
RAM
ALU RAM
18
CM
ROM
19
11
12
13

FIG. 4


14
20
EEPROM
8-BIT
ALU RAM
18
32-BIT
ECC/SHA1 BLOCK
17₁
13
ROM
12
RAM
DES BLOCK
17₂
11
CPU
TEST BLOCK
19
RF BLOCK
16

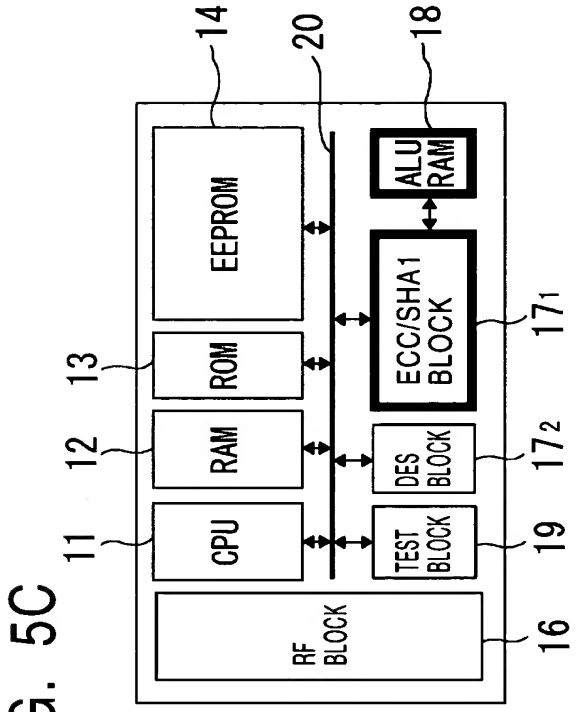


FIG. 5C

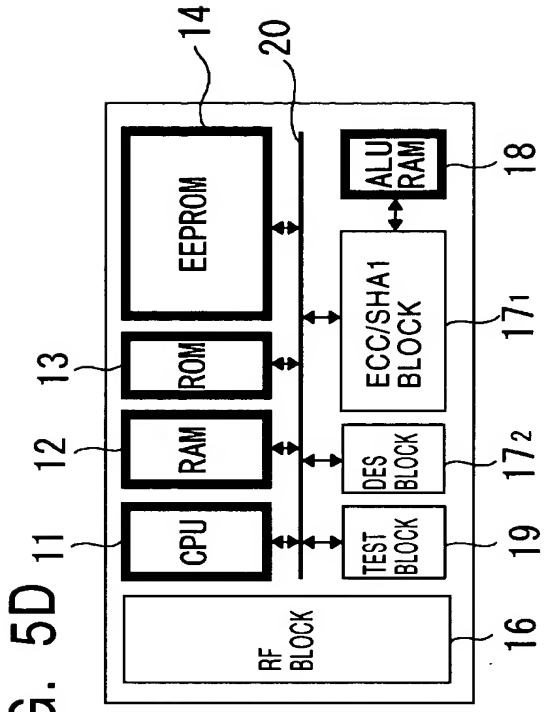


FIG. 5D

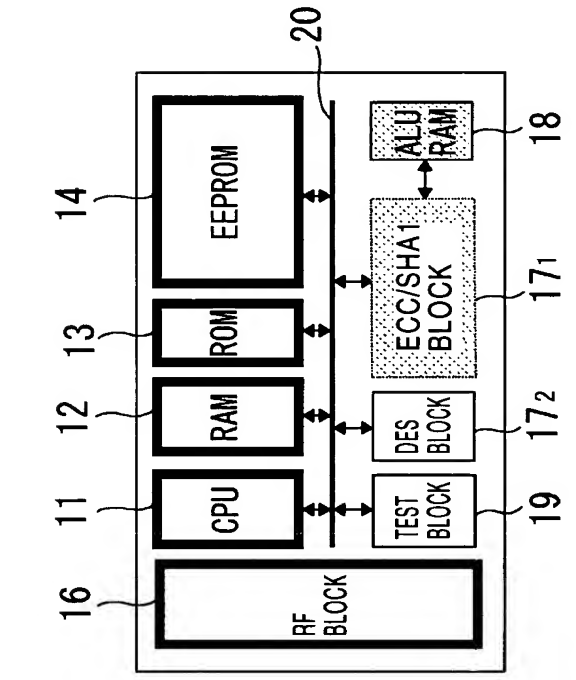


FIG. 5A

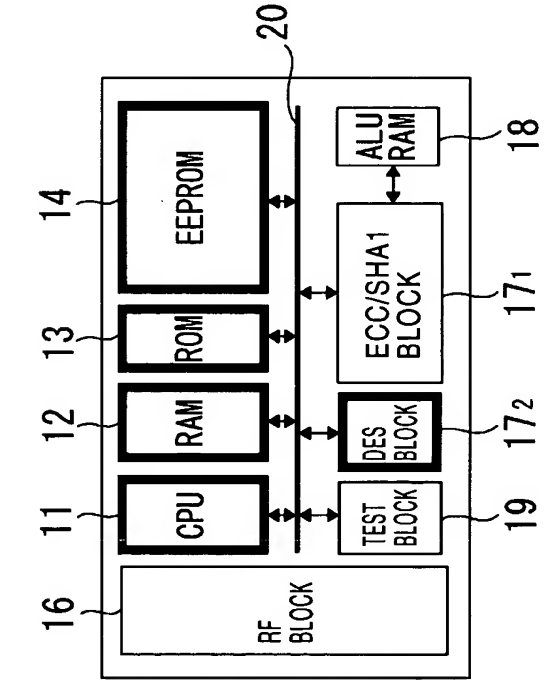


FIG. 5B

FIG. 6

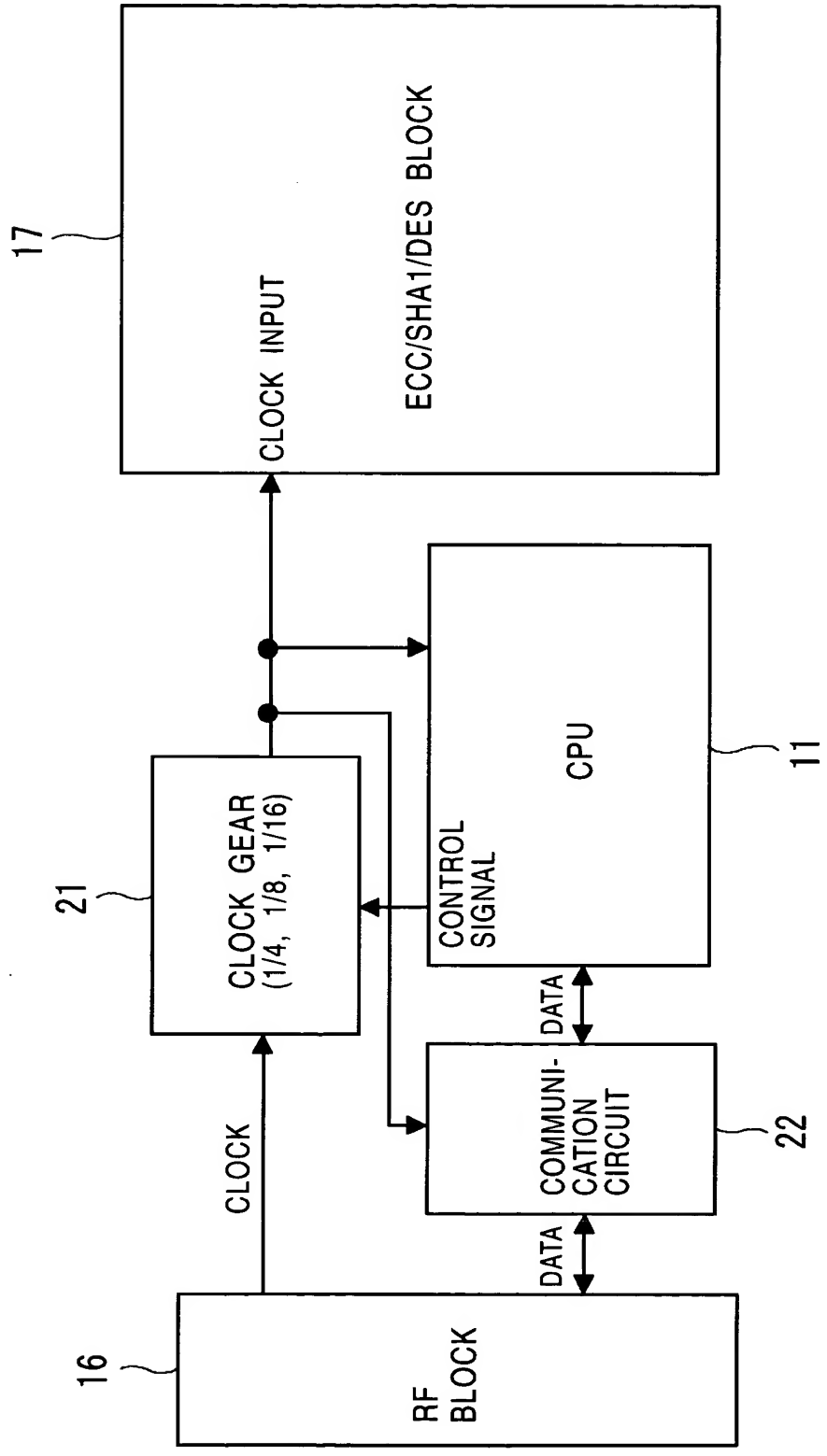

17
ECC/SHA1/DES BLOCK
CLOCK INPUT
CPU
11
CONTROL SIGNAL
21
CLOCK GEAR (1/4, 1/8, 1/16)
DATA
COMMUNI-CATION CIRCUIT
22
CLOCK
DATA
16
RF BLOCK

FIG. 7

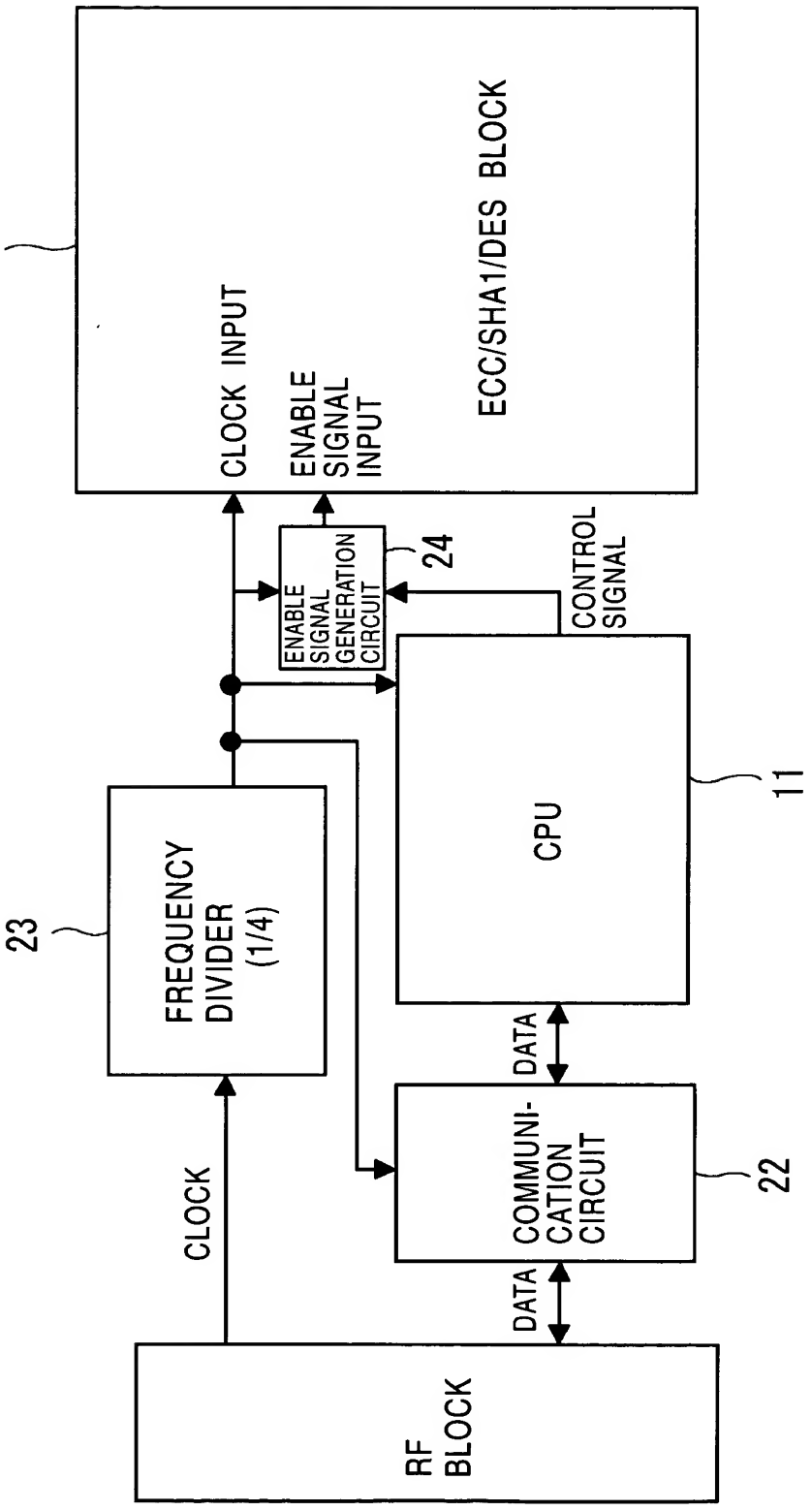
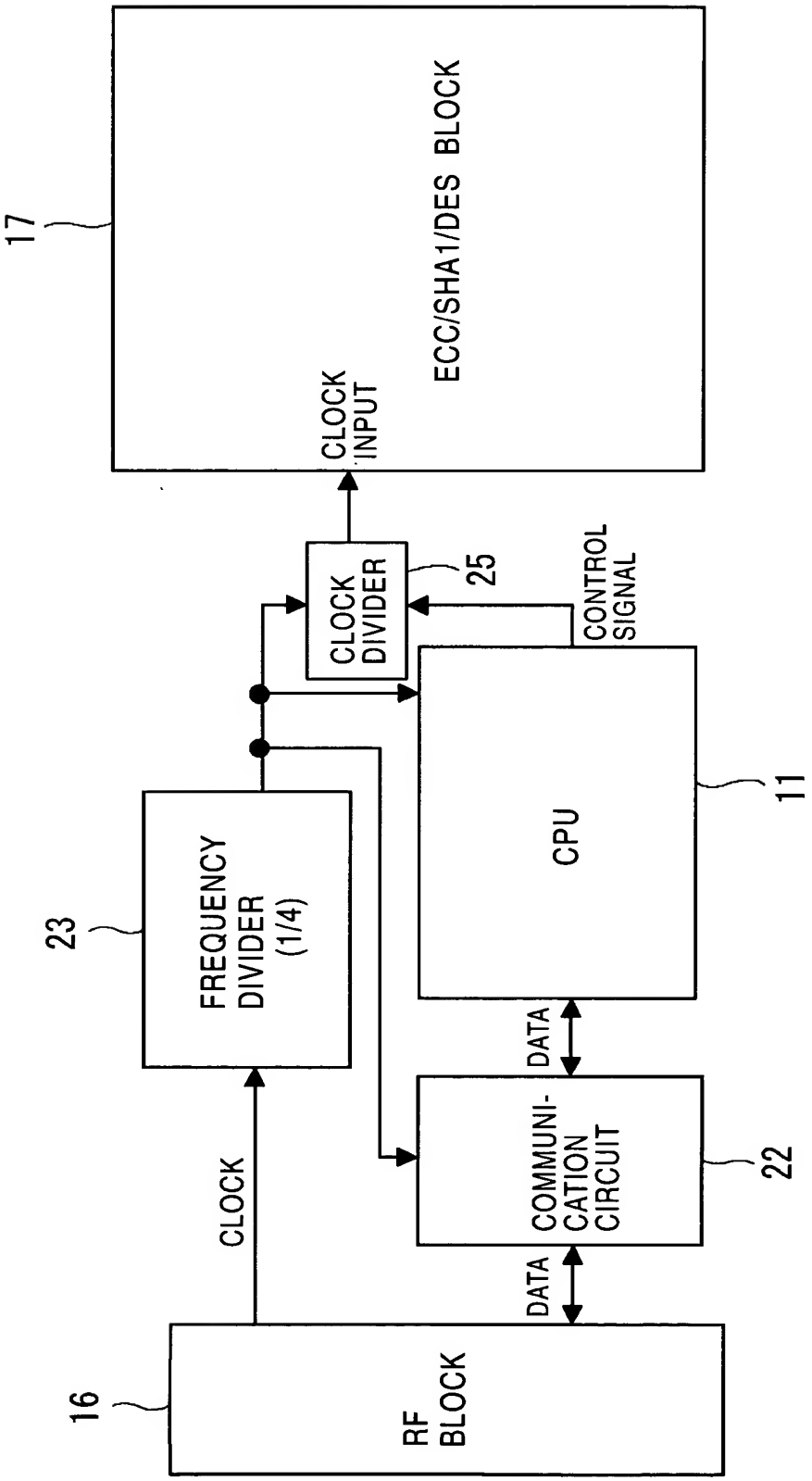

17
ECC/SHA1/DES BLOCK
CLOCK INPUT
ENABLE SIGNAL INPUT
24
ENABLE SIGNAL GENERATION CIRCUIT
CONTROL SIGNAL
CPU
11
23
FREQUENCY DIVIDER (1/4)
DATA
COMMUNI-CATION CIRCUIT
22
CLOCK
DATA
RF BLOCK

FIG. 8


17
ECC/SHA1/DES BLOCK
CLOCK INPUT
CLOCK DIVIDER
25
CONTROL SIGNAL
CPU
11
23
FREQUENCY DIVIDER (1/4)
DATA
COMMUNI-CATION CIRCUIT
22
CLOCK
DATA
16
RF BLOCK